

Notable Changes Of IS31CS8969 B0 From A1

1 Objective

The purpose of this document is to inform customers what were changed from IS31CS8969A1 to IS31CS8969B0.

2 B0 Change List

2.1 I/O Multi-Function Configuration: T0, T1, T2, T2EX

A1:

T0EN, T1EN, T2EN, T2EXEN → Not specified in the datasheet

B0:

T0EN: P2.3 enabled as Timer 0 external input → MFCFGP2.3[1]

T1EN: P2.0 enabled as Timer 1 external input → MFCFGP2.0[1]

T2EN: P2.1 enabled as Timer 2 external input → MFCFGP2.1[1]

T2EXEN: P2.2 enabled as T2EX external trigger for Timer 2 → MFCFGP2.2[1]

2.2 Added: KEY19

P1.7 can be configured as Touch Key input KEY19

2.3 Added: EUART/LIN output logic polarity

EUART_OPL: EUART/LIN output logic polarity → LININTEN[6]

EUART_OPL=0 for normal polarity.

EUART_OPL=1 will reverse the output polarity of EUART/LIN.

2.4 Slave I2C

One address register for the I2C slave controller is added. With the function of ADDR0DC(Address Bit 0 Don't Care), the slave I2C will at most respond to four different addresses where I2CSEN1 and I2CSEN2 are also set to 1. Now in IS31CS8969 B0, the user can read out I2CSADDR to know by which address the slave I2C is receiving.

2.4.1 Added: second I2C slave address I2CSADDR 2

I2CSADR2 (0xDF) I2CS2 Slave Address2 Register WO (0x00)

| | | | | | | | | |
|----|---------|-------------|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RD | - | - | - | - | - | - | - | - |
| WR | I2CSEN2 | SADDR2[6-0] | | | | | | |

I2CSEN2 Set this bit to enable the I²C slave controller.
SADDR2[6-0] 7-bit slave address.

Figure 1 I2CSADR2: I2CS2 Slave Address2 Register

2.4.2 Added: I2CSADDR read-out

I2CSADR1 (0xDD) I2CS2 Slave Address1 Register R/W (0x00)

| | | | | | | | | |
|----|---------|--------------|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RD | XMT | I2CADDR[6-0] | | | | | | |
| WR | I2CSEN1 | SADDR1[6-0] | | | | | | |

I2CSEN1 Set this bit to enable the I²C slave controller.
SADDR1[6-0] 7-bit slave address.
I2CADDR[6-0] Received slave I2C address
XMT This bit is set by the controller when the I²C slave is in transmit operation; is clear when the I²C slave controller is in receiving operation.

Figure 2 I2CSADR1: I2CS2 Slave Address1 Register

2.5 Added: LVD hysteresis auto-set

When LVDHYS[7] =1, a new threshold defined by LVDHYS[6-0] will replace the previous threshold LVDTHD[6-0] once LVD is asserted. Generally, hysteresis requires LVDHYS[6-0] to be set a higher value than LVDTHD[6-0].

LVDHYS (A016h) Supply Low Voltage Detection Threshold Hysteresis Register WO 00000000 TB Protected

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----|---------|---------|---------|---------|---------|---------|---------|---------|
| RD | LVDHYEN | LVDHYS6 | LVDHYS5 | LVDHYS4 | LVDHYS3 | LVDHYS2 | LVDHYS1 | LVDHYS0 |
| WR | LVDHYEN | LVDHYS6 | LVDHYS5 | LVDHYS4 | LVDHYS3 | LVDHYS2 | LVDHYS1 | LVDHYS0 |

Figure 3 LVDHYS: LVD Threshold Hysteresis Register

2.6 **IFB: 0x2b-0x2c Temperature Offset LSB/MSB test by ADC uses VDDH(5V) as ADC full-scale reference.**

3 **Compatibility and Influences**

1. IS31CS8969A1 and IS31CS8969B0 are pin-to-pin compatible.
2. If T0, T1, T2, T2EX external input functions might be used in A1 software, the user needs to adjust the software for running on B0.
3. If A1 software used LININTEN, for B0 it shall be checked that the value of EUART_OPL does not cause malfunction of LIN.
4. As for the other changes of B0, there is no need to modify previous A1 software.

4 **Revision History**

4.1 **V1.0**

1. First release.
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3. Release Date : 2016/08/19
4. Prepared by: Huang_jy , Checked by: Lin_ly, Approved by : Chung_yc
5. Issued by: Huang_jy

V1.1

1. Modify CS8969 to IS31CS8969.
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4. Prepared by: Huang_jy , Checked by: Liu_yl, Approved by : Chung_yc
5. Issued by: Huang_jy

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